REMARKS

The present application was filed on July 15, 2003, with claims 1-19, all of which remain pending. Claims 1, 18 and 19 are the originally-filed independent claims.

Claim 12 is objected to and claims 9 and 16 are rejected under 35 U.S.C. §112, first paragraph, due to informalities related to antecedent basis.

Claim 19 is rejected under 35 U.S.C. §101 as being directed to non-statutory subject matter.

Claims 1-5, 7, 10-11 and 14-19 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,028,847 (hereinafter "Beanland").

Claim 6 is rejected under 35 U.S.C. §103(a) as being unpatentable over Beanland in view of U.S. Patent No. 6,208,643 (hereinafter "Dieterich").

Claims 8 and 9 are rejected under 35 U.S.C. §103(a) as being unpatentable over Beanland in view of U.S. Patent No. 6,262,976 (hereinafter "McNamara").

Claims 12 and 13 are indicated as containing allowable subject matter but are objected to as being dependent upon a rejected base claim.

In this response, Applicants amend claims 7, 9, 12, 16 and 19 and add new claims 20 and 21. Applicants respectfully request reconsideration of the present application in view of the amendments above and remarks below.

Regarding the objection to claim 12 found in the first paragraph of page 2 of the present Office Action, Applicants have amended claim 12 in the manner suggested by the Examiner.

Regarding the rejections under 35 U.S.C. §112, first paragraph, of claims 9 and 16 found in the fourth, fifth and sixth paragraphs of page 2 of the present Office Action, Applicants have amended claims 9 and 16 so as to provide an appropriate antecedent basis for each recited limitation.

Regarding the §101 rejection of claim 19, Applicants respectfully traverse on the ground that the originally-recited article of manufacture comprising a storage medium containing one or more software programs, which when executed implement one or more steps producing a concrete, useful, and tangible result, constitutes a proper claim of statutory subject matter rather than "non-statutory functional descriptive matter." See, e.g., In re Beauregard, 53 F.3d 1583; 35 USPQ2d 1383 (Fed. Cir. 1995); In re Lowry, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994). Notwithstanding the traversal, Applicants have amended independent claim 19 without prejudice, solely in order to expedite prosecution of the application by conforming the claim to the preference indicated by the Examiner.

Regarding the note regarding the term "adaptable for" in claim 7, found in the second paragraph of page 4 of the present Office Action, Applicants have amended claim 7 so as to remove this term.

Applicants have added new independent claims 20 and 21, which contain limitations similar to those of allowable dependent claims 12 and 13. These claims are believed to be supported by the specification and allowable for at least the reasons discussed in the last paragraph of page 10 of the instant Office Action. As noted in the present specification at, for example, page 12, lines 19-22 and page 12, line 28 to page 13, line 4, the traffic file format disclosed herein may be advantageously used in conjunction with traffic generation methods other than that of claim 1. Furthermore, these claims recite a computer-readable medium containing functional descriptive material in the form of one or more data structures and are thus statutory under 35 U.S.C. §101 as interpreted by the Federal Circuit in In re Lowry, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994) and by the USPTO in MPEP §2106.01.

With regard to the §103(a) rejections, Applicants first note that, as discussed extensively in MPEP § 2143.03, it is well-established that an obviousness rejection requires that "all the claim limitations must be taught or suggested by the prior art." Applicants submit that the combined references fail to teach or suggest all of the limitations of claim 1.

Independent claim 1 is directed to a method of generating data traffic in a traffic generator. This method comprises the steps of generating a plurality of traffic flows and associating each of the traffic flows with at least one of a plurality of output interfaces of the traffic generator such that each of at least a subset of the plurality of output interfaces has two or more of the traffic flows associated therewith.

In an illustrative embodiment shown in FIGS. 1 and 2 and described in the specification at, for example, page 6, line 16 to page 7, line 9 and at page 8, lines 23-26, traffic generator 100 is configured to generate a plurality of traffic flows 200. Each of the traffic flows is associated with at least one of a plurality of output interfaces 202 such that each of at least a subset of the plurality of output interfaces has two or more of the traffic flows associated therewith. In the illustrative embodiment shown in FIG. 2 and described in the specification at page 7, lines 4-4, Traffic Flow (1), Traffic Flow (2) and Traffic Flow (i) are associated with output interface 202-1.

Beanland, on the other hand, teaches a conventional arrangement with only a single output interface. See, for example, Beanland at column 7, lines 33-38 ("The cell generator 103 functions to

. . . generate output packets which are output via a synchronous interface to the instrument specific hardware interface 104 which generates the required real-time data payload for the instrument under test 106.") See also Beanland at column 8, lines 5-8 ("[T]he cell generator 103 must typically be connected to a hardware interface 104 device to interconnect the multiple stream traffic emulator 1 with the load which it drives.")

The arrangement taught in the above-noted illustrative embodiment of the claimed invention provides several advantages over the conventional arrangement taught by Beanland. For example, as discussed in the specification at, for example, page 8, lines 26-28, this illustrative embodiment advantageously allows a simulated or actual device, such as a simulated or actual network processor, to receive a wide variety of different types of user configurable data traffic via the plurality of output interfaces.

In formulating the rejection of claim 1, in the sixth paragraph of page 6 of the present Office Action, the Examiner concedes that Beanland fails to disclose the limitation recited in claim 1 wherein "each of at least a subset of the plurality of output interfaces has two or more of the traffic flows associated therewith." The Examiner instead contends:

> [i]t is well known to a person of ordinary skill in the art. Thus it would have been obvious to the person of ordinary skill in the art at the time of invention to implement a method of implementing two or more of the traffic flows in each of at least a subset of the plurality of output interfaces.

Applicants respectfully submit that this is a conclusory statement of the sort rejected by both the Federal Circuit and the U.S. Supreme Court. See KSR v. Teleflex, No. 13-1450, slip. op. at 14 (U.S., Apr. 30, 2007), quoting In re Kahn, 441 F. 3d 977, 988 (Fed. Cir. 2006) ("[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.").

It appears that the Examiner is relying on official notice in formulating this rejection; specifically, the assertion that "it is well known to the person of ordinary skill in the art" to associate two or more traffic flows with each of at least a subset of the plurality of output interfaces. Applicants respectfully note that MPEP § 2144.03 specifically states that "[i]t would not be appropriate for the examiner to take official notice of facts without citing a prior art reference where

the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well known. For example, assertions of technical facts in the areas of esoteric technology or specific knowledge of the prior art must always be supported by citation to some reference work recognized as standard in the pertinent art." (emphasis in original). Applicants respectfully submit that the application of official notice to reject claim 1, in the absence of any evidentiary showing, fails to comply with this instruction. Applicants respectfully request that, for each invocation of official notice, the Examiner provide either documentary evidence or an affidavit or declaration setting forth specific factual statements and explanation to support the finding, as required by 37 C.F.R. § 1.04(d)(2) in order for such a rejection to be maintained.

In the first paragraph on page 7, the Examiner asserts that "[t]he method for implementing two or more of the traffic flows in each of at least a subset of the plurality of output interfaces can be implemented by assigning a sequence number field in each of the data packets so that the traffic flows can be implemented by assigning a sequence number field in each of the data packets so that the traffic flows can be identified at the receiving terminal." However, as noted in MPEP § 2144.01, "the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." Thus, the Examiner's suggestion regarding a possible implementation of the claim limitation is inapposite to the question of obviousness.

Likewise, the Examiner's statement, found in the second paragraph on page 7, that "[t]he motivation for implementing two or more of the traffic flows in each of at least a subset of the plurality of output interfaces is that it reduces the number of output interfaces needed in a traffic generator, which leads to the reduction in hardware costs," fails to provide sufficient motivation. More specifically, the statement above is using the benefit obtained from a combination as a motivation for that combination; this is impermissible hindsight. In order to avoid the improper use of a hindsight-based obviousness analysis, particular findings must be made as to why one skilled in the relevant art, having no knowledge of the claimed invention, would have modified the teachings of Beanland in the manner claimed (See, e.g., In re Kotzab, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000)). The Examiner's conclusory statements do not adequately address the issue of motivation to combine references. "It is improper, in determining whether a person of ordinary skill would have been led to this combination of references, simply to '[use] that which the inventor

taught against its teacher.'" In re Sang-Su Lee, 277 F.3d 1338, 1344 (Fed. Cir. 2002) (quoting W.L. Gore v. Garlock, Inc., 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983)).

Independent claims 18 and 19 contain limitations similar to those of independent claim 1 and are thus believed to be patentable for at least the reasons identified above with regard to claim 1.

Dependent claims 2-18 are believed to be patentable for at least the reasons identified above with regard to claim 1. Additionally, one or more of these claims defines separately patentable subject matter.

For example, claim 6 recites a limitation "wherein the traffic generator is operable in at least two phases, including a first phase in which a timestamp table is constructed based at least in part on user-selected configuration information, and a second phase in which packets are generated using the timestamp table constructed in the first phase." As discussed in the specification at, for example, page 9, lines 11-19 and page 10, lines 12-20, the timestamp table preferably indicates the times at which packets should be generated in order to provide the desired traffic output.

In formulating the rejection of claim 6, the Examiner argues:

> Beanland discloses a method of generating data traffic described in paragraph 6 of this office action except the method of generating packets using a timestamp table. The invention of Dieterich et al. from the same or similar fields of endeavor teach a method of constructing a timestamp table in the memory of a processor.
>
> Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to implement the method of generating packets using a timestamp table.
>
> The method of generating packets using a timestamp table can be implemented by implementing a clock to keep track of the time of arrival of each input packets [sic] and store the data in a memory of a processor.

The statement of motivation to combine Beanland and Dieterich is deficient for at least reasons similar to those described above with regard to claim 1. Indeed, the Examiner has not only failed to indicate a cogent explanation of motivation to combine the references, but has also failed to indicate which portion of Dieterich is being relied upon, in contravention of 37 CFR § 1.104(c)(2) ("In rejecting claims for want of novelty or for obviousness, the examiner must cite the best references at his or her command. When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable.")

Applicants further submit that Beanland, which relates to "a multiple stream traffic emulator which functions to generate digital traffic," (Beanland at column 1, lines 6-7) (emphasis supplied) and Dieterich, which "relates to an apparatus and concomitant method for measuring the parameters of received digital bitstreams," (Dieterich at column 1, lines 7-9) (emphasis supplied) are not analogous art; Beanland is directed toward generation of digital bitstreams and Dieterich toward analysis of received digital bitstreams.

Furthermore, the timestamp table disclosed in Dieterich does not teach or suggest that recited in claim 6, which indicates both that the "timestamp table is constructed based at least in part on user-selected configuration information" and that "packets are generated using the timestamp table." Dieterich, on the other hand, in fact teaches away from these limitations by instead defining a timestamp table as a "list of times of receipt of packets" (column 5, line 8) and teaching that "software applications or methods executing in processor 240 use the values in the timestamp table 252 to process a packet's data stored in buffer 210 and evaluate its time elements in the context of its time of reception." (column 5, lines 24-28). Additionally, neither Beanland nor Dieterich, alone or in combination, teach or suggest the limitation of claim 6 wherein "wherein the traffic generator is operable in at least two phases," much less the specific phases recited.

Likewise, claims 8 and 9 recite limitations "wherein the traffic generator comprises a sequencer having a plurality of user-selectable sequencing processes associated therewith, a given one of the sequencing processes specifying an order of selection of items from a configuration list" and "wherein the plurality of sequencing processes comprises a group sequencer which provides a correlative mapping between two or more configuration lists and their associated parameters."

As discussed in the present specification at, for example, page 10, lines 1-9, an illustrative embodiment of this sequencer specifies an order of selection of items from a configuration list, which in turn is defined in the present specification at page 9, lines 22-28, as comprising a list of any desired number of values corresponding to a given configurable parameter. Examples of sequencing processes that may be supported by the sequencer include round robin, random, weighted random, weighted indexed round robin, and user-defined ordering.

As discussed in the specification at, for example, page 10, lines 5-9, the sequencer recited in claim 8 may be advantageously used in conjunction with the generation of traffic designed to stress test scheduling algorithms associated with the provision of class of service or quality of service (QoS) performance in a given system. The group sequencer recited in claim 9 allows correlation of

two or more parameters having the same number of values in the configuration list, thereby providing a definitive mapping between different parameters.

In formulating the rejection of claims 8 and 9, the Examiner concedes that Beanland fails to disclose the limitations of claims 8 and 9, but instead argues that the "invention of McNamara from the same or similar fields of endeavor teaches different types of sequencing processes (see column 13 lines 19-30)." The relied-upon portion of McNamara states that:

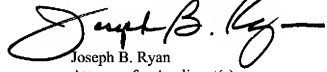
> This numbering sequence identifies the most connected interior routers by low numbers followed by the least connected interior routers, and finally the highest numbered routers are exterior domain routers. This number also has the following properties: the lower the number of a router the greater the influence on interior traffic; and conversely the higher the number of a router the greater the influence on transitory traffic. It should be appreciated that the numbering sequence direction is somewhat arbitrary, in that one can instead number from high interior numbers to low exterior numbers. The importance is the sequencing and not the numeric direction of the sequence.

Applicants respectfully submit that this fails to teach or suggest the limitations of claims 8 and 9. Instead, it disclosing a numbering sequence indicative of the influence of a given router on traffic.

Additionally, the statement of motivation to combine Beanland and McNamara is deficient for at least reasons similar to those described above with regard to claim 1. Furthermore, Beanland and McNamara are non-analogous art for at least reasons similar to those described above with regard to claim 6.

In view of the foregoing, claims 1-21 as amended are believed to be in condition for allowance.

Respectfully submitted,



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